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DESIGN • PRODUCTION • ASSEMBLY

System-on-a-Chip: closing the test gap

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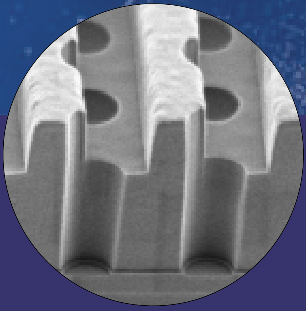

Sub-0.18 µm damascene etch schemes

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Optimising CVD through RF metrology

Intel's ex-Digital Equipment fab describes how application of RF monitoring for real-time process control, excursion detection and clean optimisation to a PECVD wafer processing tool can reduce test wafers, spare part usage and tool downtime, while increasing yield and throughput.

Table 1: Time savings to be gained from using an RF end-point system compared to the standard timed cleans.

	Av. timed duration	1st RF endpoint	Endpoint+ 20% overetch	Time saved	% saving
SACVD single-step	57.17 s	31.50 s	37.80 s	19.37 s	33.88%
PECVD single-step	95.12 s	57.51 s	69.01 s	26.11 s	27.45%
SACVD+PECVD single-step	–	–	–	45.48 s	29.86%
PECVD two-step	270.69 s	121.57 s	145.88 s	124.81 s	53.89%

A PECVD tool is used in semiconductor manufacturing to deposit a variety of dielectric (insulator) layers. A common configuration is a multi-chamber platform consisting of a loadlock chamber and up to four additional process chambers. Each process chamber processes one wafer at a time, and there are a variety of process chambers that can be mounted on the loadlock. The chamber type this paper deals with is a universal chamber.

The process used in this particular universal chamber consists of two different depositions, and their corresponding chamber cleans:

- phosphorus-doped silicon oxide sub-atmospheric chemical vapour deposition (SACVD) followed by a corresponding chamber clean;
- phosphorus-doped silicon oxide plasma-enhanced chemical vapour deposition (PECVD), also followed by a chamber clean.

The PECVD deposition begins with a stabilisation step, where the process gases or chemicals, in this case TEOS (Tetraethylorthosilicate), TEPO (Triethylphosphate) and oxygen, begin flowing, and the chamber pressure stabilizes. In the next step, RF (radio frequency) power is supplied to the electrode, a plasma ignites, and the dielectric film is deposited on the wafer. The stability and reproducibility of the plasma is critical to dielectric film properties and subsequent product yield.

As the dielectric film is deposited on the wafer, it is also deposited on the walls of the chamber and the process kit hardware. This film needs to be removed from the chamber walls and hardware before the next wafer is processed otherwise it can jeopardise the on-wafer uniformity and thickness, as well as the on-wafer particle levels.

This film removal is accomplished with a chamber clean. The first step is again a stabilisation step, where the process gases are introduced - in this case C_2F_6, O_2 and NF_3 - and the chamber pressure stabilises. In the next step, the RF power is applied, igniting a plasma that etches away the dielectric film deposited on the walls and process kit.

The SACVD process differs from the PECVD process in that it does not use RF power during the deposition phase, and it uses O_3 instead of O_2. The corresponding chamber clean differs from the PECVD process chamber clean in that it has an additional throttle-valve clean step, and its clean time is slightly different.

- *RF MONITORING SYSTEM:*

To monitor the plasma, an RF sensor is used in Fourth State Technology's RFMS (designed at SEMATECH for application to the PECVD tool), which is installed in-line between the impedance-matching network and powered electrode. This sensor contains current and voltage transducers and is designed to survive the harsh conditions at the powered electrode without inducing process shifts in key process parameters. Shielded cables carry the voltage and current signals from the RF sensor to a base unit which houses the RF electronics designed to filter and analyse the RF signal. Measurements are made of the first five harmonics of voltage and current and the phase angle at the fundamental frequency.

FST's process control software makes use of the RF voltage and current spectral information to evaluate process performance. Process control is achieved using three main modules: trend analysis, excursion detection and endpoint detection. All three modules can be employed in real time for maximum performance improvement:

- Endpoint detection module:

Endpoint refers to the point at which a process chamber is completely clean and the clean process can be terminated. During clean, the chamber impedance changes as the process by-products are removed from the chamber walls and surfaces. Depending on the composition of the by-products, and the process used to remove them, the chamber impedance either increases or decreases until all of the by-products are removed.

Once all by-products are removed from the chamber, the impedance (and thus voltage, current and phase angle) stabilises. Consequently, a chamber clean endpoint can be detected using the voltage, current or phase-angle signals.

With the FST endpoint package, the user can develop an algorithm using one of the 11 signals collected, to provide real-time chamber clean endpointing.

- FST's "Go-No-Go" package, designed for excursion detection: In this module, the user enters reference values and warning and alarm limits for the mean, range and standard deviation of the 10 voltage and current signals. The module monitors these signals and - if the limits are exceeded - provides warnings and alarms in real-time, displayed on the PECVD tool's human interface.

Process shifts and mechanical failures in the tool will often voltage and current signals to shift. By establishing limits for the different signals, the user can receive warnings and alarms. FST has developed a simple implementation strategy for determining these limits.

- Trend analysis package: useful to understand long-term transients in the process tool performance such as wet clean cycles and transitions in film stress. FST's SPC module makes use of standard Western Electric control chart rules as well as customised versions to provide real-time, run-by-run process control. ➤

THE PECVD OPTIMISATION APPLICATION

This application focused on the Endpoint and "Go-No-Go" capabilities of the RFMS unit:

- The Endpoint capability was used to compare single-step and two-step chamber cleans, and provide information on clean time optimisation.
- The "Go-No-Go" capability was used to investigate test wafer reduction, excursion detection and equipment troubleshooting.

• *ENDPOINT APPLICATION*

Initially an RFMS unit was installed on two process chambers for passive endpoint monitoring. One chamber used a single-step timed, chamber clean. The other chamber used a two-step timed, chamber clean.

Several thousand chamber clean endpoint traces were collected from both chambers with the RFMS unit. Sample endpoint traces of the single-step PECVD and SACVD chamber cleans are shown in Figure 1. Sample end-point traces of the inner and outer cleans of the two-step, PECVD chamber clean are shown in Figure 2.

Figure 1 shows that the single step chamber cleans had distinct, repeatable, endpoints.

Figure 2 shows that the inner cleans (first step) of the two-step cleans, had distinct, repeatable, endpoints. However, the outer cleans (second step) show no visible endpoint. The chamber clean reached endpoint during the inner clean step of the two-step clean - the entire chamber and kit hardware was clean before the end of the inner step. The outer clean was therefore not necessary, and was consuming substantial amounts of clean gases and causing undue wear on hardware, a known cause of yield limiting particles.

Figures 1 and 2 also show the differences between RF based endpoint times versus the duration of the timed cleans. It was determined that the chamber clean times could be greatly reduced, cutting process gas consumption and wear on process kits. Reducing chamber clean time also reduces RF hours on the chamber, which should result in extending time periods between wet cleans. Fewer wet cleans translates to less tool downtime and increased tool throughput.

Table 1 shows the time savings to be gained using an RF endpoint system as opposed to the standard timed cleans.

Based on the reduced clean times and RF hours resulting from RF endpoint, yearly savings were calculated which determined the amount of gas saved due to reduced clean times and the number of process kits saved by the reduced RF hours. Figure 4 shows the results of these calculations.

(Note: All specific process parameters have been removed.)

Fig 1: Traces for single-step chamber cleans show repeatable distinct end-points for (left) PECVD and (right) SACVD.

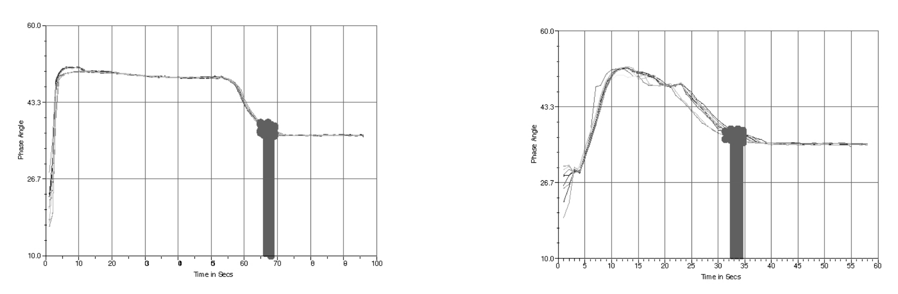
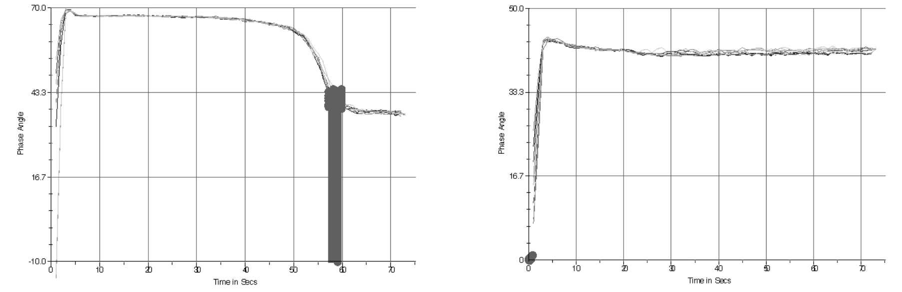


Fig 2: Traces for (left) inner and (right) outer PECVD chamber clean steps show repeatable, distinct end-points.



• *"GO-NO-GO" APPLICATION*

The RFMS unit collected data on the deposition steps during the same time period that is was collecting the endpoint data on the chamber cleans.

Over 800 data files from each chamber were collected from the depositions. The mean, range and standard deviation for each of the ten voltage and current signals were calculated automatically in real-time by the process control software and used to establish reference values and warning and alarm limits for each of the signals.

During the start-up phase for the "Go-No-Go" application, data was reviewed to determine the potential to detect process shifts or equipment failures leading to undesirable wafer results. During this application two equipment problems resulting in process excursions, occurred. One chamber experienced a helium (TEOS) regulator failure. This regulator failure was detected by the RFMS unit, triggering range alarm limits for the V0 and V2 signals. Figure 5 shows the V0 output trace for one of the files that alarmed

Fig 3: Trace of V0 prior to HE (TEOS) regulator fault (left - excursion takes approximately 10 seconds to recover) and afterwards (right - no large signal drops).

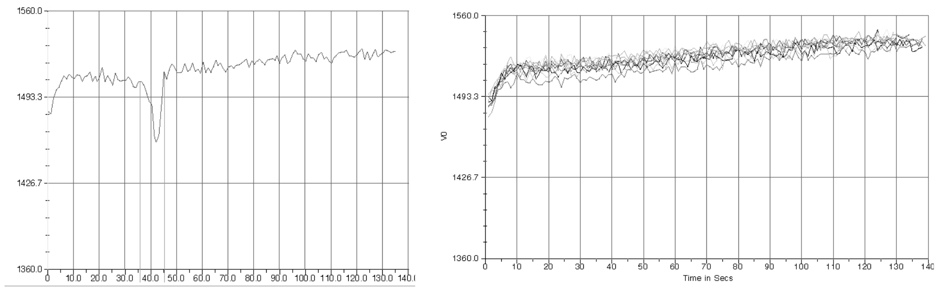


Fig 4: Example of V1 trace: (left) micro-arcing, particle problem - excursion takes about 5 s to recover); (right) after wet clean - no large voltage drops.

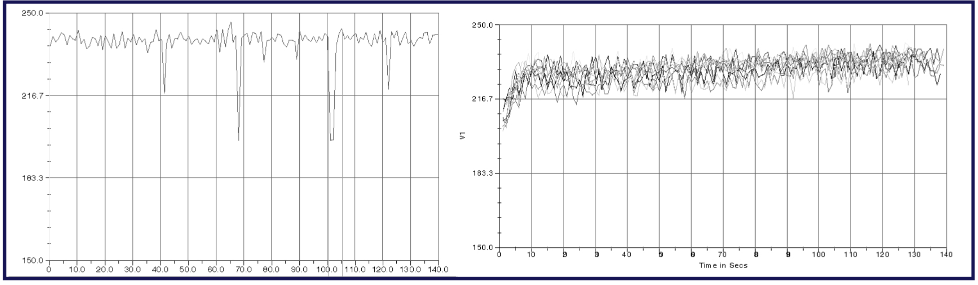


Fig 5: Measured film stress vs FST predicted film stress.

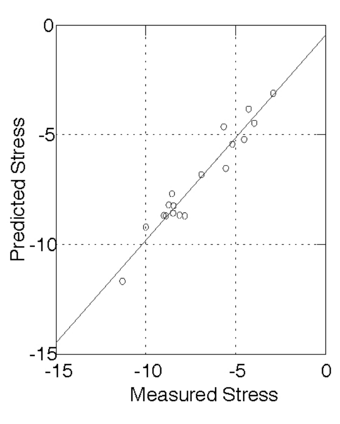
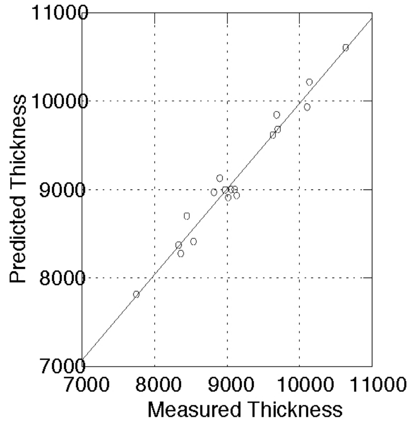


Fig 5: Measured film thickness vs FST predicted film thickness.



for the regulator failure, showing a large drop in the voltage signal that takes approximately 10 seconds to recover. This type of signature is typical of flow or pressure fluctuations. It should be noted that the actual flow fault was a short transient. However, the resulting plasma relaxation time was substantial.

After the regulator was replaced, there were no further alarms. Figure 6 shows a sample of the V0 output traces without regulator problems. The figure also shows no large voltage drops throughout the traces. Similar results were seen with the V2 output traces.

While running chamber characterisation monitors, the second chamber that was monitored experienced an episode of extremely high particle counts. This problem was also detected and documented by the RFMS, which triggered range alarm limits for the V1 signal.

Figure 7 shows the V1 output trace for one of the files that alarmed for the particle problem. This shows several large drops in the voltage signal, that take two to three seconds to recover. This type of signature is very typical of micro-arcing in the chamber, which often generates particles. The chamber was wet cleaned eliminating the arcing problem.

Figure 8 shows no large voltage drops in the V1 output traces after the chamber was wet-cleaned.

A more severe arcing problem will exhibit itself as much larger drops in all five voltage signals. Severe arcing has the potential to damage devices and cause serious yield loss.

The final part of the "Go-No-Go" analysis was a designed experiment (DOE). The DOE was used to determine the correlation between the 11 signals collected by the RFMS unit, and the process tool parameters and wafer results. The DOE was a Box-Behnken design using eighteen wafers. The adjusted variables were pressure, power and gap spacing. The adjusted range of variables was 10%. The RFMS unit collected RF data during the DOE and all wafers were measured for stress and thickness. Upon completion of the DOE, the data was analysed to create models for predicting wafer results and improving process parameters.

Table 2 shows the DOE model summary. These represent linear models using FST parameters as predictors. The table shows that the film stress and film thickness wafer results can be predicted at a high confidence level. The process parameters of RF power, electrode spacing and pressure can also be predicted at a high confidence level.

Figure 9 is a plot of the predicted film stress versus the actual measured film stress. One can see close agreement between the model prediction and the measured values.

Figure 10 is a plot of the predicted film thickness versus the actual measured film thickness. As in the case of the stress model, the thickness model was quite close to actual measurement across the design space. This presents an opportunity to use in-situ RF measurements to confirm or replace expensive wafer tests.

RESULTS AND CONCLUSIONS

In this evaluation, Digital Equipment Corporation* successfully optimised their PECVD and SACVD processes in terms of reducing manufacturing cost, throughput and yield. Using a Fourth State Technology RFMS unit, it was verified that a single-step chamber clean could successfully replace the two-step chamber clean. The RFMS unit showed that the process chamber and hardware were completely clean, reaching endpoint before the end of the inner step of the two-step chamber clean.

It was also determined that the single-step clean time could be greatly reduced. Moving from the two-step chamber cleans to single-step chamber cleans greatly reduces clean times. This time reduction results in reduced gas consumption of costly clean gases. It also reduces the RF hours the chamber experiences, extending kit life and tool throughput and reducing preventive maintenance events and tool downtime. The times were also reduced on the single-step chamber cleans; further reducing gas consumption and tool downtime and increasing kit life and tool throughput.

Table 2: Designed experiment model summary.

Response	Model terms	Ajd R-square
Film stress	V0, V3, I0	0.920
Film thickness	V2, I0, I2	0.961
Uniformity	V2, I0, I2	0.738
RF power	V1, I0, phase	0.986
Electrode spacing	V2, V3, I0, I3	0.932
Pressure	V0, I0, I2	0.959

The "Go-No-Go" portion of this evaluation revealed several substantial applications of the RFMS unit for process control and measurement wafer reduction. Digital Semiconductor was able to detect two different processing faults with the RFMS unit; a Helium regulator failure, and a gross particle failure during chamber characterisation runs. With the aid of a simple designed experiment, Digital Semiconductor was also able to identify the RF parameters which correlated to excursions in RF power, electrode spacing and pressure, as well as stress and thickness wafer measurements. These correlations provide not only detection capability, but also valuable troubleshooting information. In conclusion, all goals of process optimisation, process control and excursion detection established for this application were met.

As a result of this evaluation, Digital Semiconductor has moved all post-deposition cleans to single-step cleans for both doped and undoped films. Also, all doped film chamber cleans have been evaluated and post deposition clean times optimised using FST RFMS equipment. Overall, "On Product" particle counts have seen a measurable improvement, and "Plasma On" time during chamber cleans has been reduced by 30%. A further FST evaluation has been planned for Digital Semiconductor's undoped chambers with the expectation of additional process optimisation.

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